Notice of Allowability	Application No.	Applicant(s)	
	10/765,420	BHAKTA ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *19 November 2004 and 16 February 2005*.

2. ☒ The allowed claim(s) is/are *1,2,5-9,11-13,15-18 and 20*.

3. ☒ The drawings filed on *27 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 111904
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

HOAI HO
PRIMARY EXAMINER

DETAILED ACTION

1. Applicant's Amendment filed November 19, 2004 has been entered. Claims 1, 8, 17, and 20 have been amended. Claim 3 has been cancelled.

2. Applicant's Information Disclosure Statement, IDS, filed November 19, 2004 has been considered by the Examiner.

3. This application is in condition for allowance except the following formal matter.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Bruce S. Itchkawitz (reg. no. 47,677) on February 16, 2005.

The application has been amended as follows:

i. **Claims 4, 10, 14, and 19 are further cancelled.**

ii. **Replace claims 1, 5 – 8, 11 – 13, 15 – 17, and 20** with the following revised and amended version.

1. A memory module comprising:

a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a

line of bilateral symmetry substantially perpendicular to the edge and which bisects the printed circuit board into a first lateral half and a second lateral half, the printed circuit board having a plurality of interconnection levels;

a first row of integrated circuits identical to one another, the first row mounted on the first side of the printed circuit board, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction;

a second row of integrated circuits identical to the integrated circuits of the first row, the second row mounted on the first side of the printed circuit board, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is the first row, the integrated circuits of the second row having a second orientation direction different from the first orientation direction;

a first register connected to the integrated circuits of the first row and the second row on a first lateral portion of the printed circuit board by a first set of address signal paths;

a second register connected to the integrated circuits of the first row and the second row on a second lateral portion of the printed circuit board by a second set of address signal paths;

a first plurality of data lines electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area, each data line

of the first plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length; and

a second plurality of data lines electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area, each data line of the second plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length, each data line having a length substantially equal to a sum of the trace portion lengths of the data line, whereby lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same.

5. The memory module of claim 1, wherein the first row is bilaterally symmetric with respect to the line of bilateral symmetry.

6. The memory module of claim 1, wherein the second row is bilaterally symmetric with respect to the line of bilateral symmetry.

7. The memory module of claim 1, wherein the first set of address signal paths and the second set of address signal paths are bilaterally symmetric to one another across the line of bilateral symmetry.

8. A method for arranging integrated circuit locations on a printed circuit board for a memory module, the method comprising:

providing a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a line of bilateral symmetry substantially perpendicular to the edge and which bisects the printed circuit board into a first lateral half and a second lateral half, the printed circuit board having a plurality of interconnection levels;

mounting a first row of integrated circuits identical to one another on the first side of the printed circuit board, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction;

mounting a second row of integrated circuits on the first side of the printed circuit board, the integrated circuits of the second row identical to the integrated circuits of the first row, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is the first row, the integrated circuits of the second row having a second orientation direction different from the first orientation direction;

electrically connecting a first register to the integrated circuits of the first row and the second row on a first lateral portion of the printed circuit board by a first set of address signal paths;

electrically connecting a second register to the integrated circuits of the first row and the second row on a second lateral portion of the printed circuit board by a second set of address signal paths;

electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area by a first plurality of data lines, each data line of the first plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length; and

electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area by a second plurality of data lines, each data line of the second plurality of data lines comprising trace portions on different interconnection levels of the printed circuit board, each trace portion having a trace portion length, each data line having a length substantially equal to a sum of the trace portion lengths of the data line, wherein lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same.

11. The method of claim 8, wherein the first row is bilaterally symmetric with respect to the line of bilateral symmetry.

12. The method of claim 8, wherein the second row is bilaterally symmetric with respect to the line of bilateral symmetry.

13. The method of claim 8, wherein the first set of address signal paths and the second set of address signal paths are bilaterally symmetric to one another across the line of bilateral symmetry.

15. The method of claim 8, wherein the first lateral portion comprises the first lateral half.

16. The method of claim 8, wherein the second lateral portion comprises the second lateral half.

17. A memory module comprising:

a printed circuit board having an edge, a first side, and a common signal trace connector area positioned along the edge, the printed circuit board having a line of bilateral symmetry substantially perpendicular to the edge and which bisects the printed circuit board into a first lateral half and a second lateral half, the printed circuit board having a plurality of interconnection levels;

a first row of integrated circuits identical to one another, the first row mounted on the first side of the printed circuit board, the first row being substantially parallel to the edge and in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction;

a second row of integrated circuits identical to the integrated circuits of the first row, the second row mounted on the first side of the printed circuit board, the second row being substantially parallel to the edge and in proximity to the first row and located physically farther from the common signal trace connector than is the first row, the integrated circuits of the second row having a second orientation different from the first orientation direction;

a first register and a second register;

means for connecting the first register to the integrated circuits of the first row and the second row on a first lateral portion o the printed circuit board;

means for connecting the second register to the integrated circuits of the first row and the second row on a second lateral portion of the printed circuit board; and

means for electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area via different interconnection levels of the printed circuit board and for electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area via different interconnection levels of the printed circuit board, whereby corresponding trace lengths to the first row of integrated circuits and the second row of integrated circuits are substantially the same.

20. The memory module of claim 17, wherein the means for connecting the first register to the integrated circuits of the first row and the second row on the

first lateral portion is bilaterally symmetric across the line of bilateral symmetry to the means for connecting the second register to the integrated circuits of the first row and the second row on the second lateral portion.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
February 16, 2005

HOAI HO
PRIMARY EXAMINER